

WHAT IS CLAIMED IS:

- 1 1. An integrated circuit comprising:
2 a differential amplifier having a first input coupled to a pad of the integrated
3 circuit and a second input coupled to a reference voltage;
4 a pull-up transistor coupled between a supply voltage and the pad; and
5 a logic gate having an output coupled to a control electrode of the pull-up
6 transistor and an input coupled to an output of the differential amplifier.
- 1 2. The integrated circuit of claim 1 wherein a voltage output high level at
2 the pad will be the lesser of the reference voltage level or the supply voltage.
- 1 3. The integrated circuit of claim 1 wherein the differential amplifier
2 outputs a logic one when a voltage level at the pad is greater than a voltage level of the
3 reference voltage.
- 1 4. The integrated circuit of claim 1 wherein the reference voltage is less
2 than the supply voltage.
- 1 5. The integrated circuit of claim 1 further comprising:
2 a leaker device coupled to the pad to statically hold the pad at a desired VOH
3 level or above.
- 1 6. The integrated circuit of claim 5 wherein a control electrode of the
2 leaker device is coupled to a leaker reference voltage which is generated on-chip.
- 1 7. The integrated circuit of claim 5 wherein a control electrode of the
2 leaker device is coupled to a supply voltage.
- 1 8. The integrated circuit of claim 1 further comprising:
2 a voltage reference generator circuit, coupled to the second input of the
3 differential amplifier, to generate the reference voltage.
- 1 9. The integrated circuit of claim 1 wherein the reference voltage is
2 provided by way of an external source coupled to a pad of the integrated circuit.

- 1 10. The integrated circuit of claim 1 wherein the logic gate performs an
2 OR function.
- 1 11. The integrated circuit of claim 1 further comprising:
2 logic array blocks, configurable to implement user-logic functions, providing
3 a logical output coupled to another input of the logic gate.
- 1 12. The integrated circuit of claim 1 wherein the pad is also coupled to an
2 input buffer circuit.
- 1 13. The integrated circuit of claim 8 wherein the voltage reference
2 generator is programmable to select a level of the reference voltage.
- 1 14. The integrated circuit of claim 8 wherein the voltage reference
2 generator is programmed before the integrated circuit is used for normal operation.
- 1 15. The integrated circuit of claim 8 wherein the voltage reference
2 generator is programmable to select from a plurality of reference voltage levels.
- 1 16. The integrated circuit of claim 1 wherein the supply voltage is a noisy
2 VCC supply voltage.
- 1 17. The integrated circuit of claim 1 wherein the integrated circuit is a
2 programmable logic integrated circuit.
- 1 18. The integrated circuit of claim 1 wherein the pull-up transistor
2 dynamically holds the pad at a voltage output high level.
- 1 19. The integrated circuit of claim 1 further comprising:
2 a standard I/O buffer circuit coupled to the pad, wherein the standard I/O
3 buffer circuit provides support for voltage output high levels compatible with the supply
4 voltage, and the pull-up transistor, differential amplifier, and logic gate provide support for
5 voltage output high levels compatible with voltages other than the supply voltage.

1 20. The integrated circuit of claim 1 wherein the pull-up transistor is a
2 PMOS device.